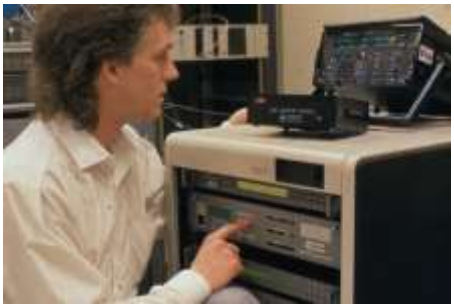

Peter Johnson – Submitted on 9/9/2026

Walking through the doors of Comsat Laboratories in Clarksburg, Maryland, in August of 1981 - the start of what would become a thirteen-year chapter of my life - I began on the ground floor as a technician. It was the golden age of satellite communications engineering, a place where problems were solved at the physical layer with solder, wire wrap, and raw ingenuity. Over those thirteen years, I grew from spinning a wire-wrap tool and troubleshooting breadboards into a full-fledged engineer, driven by a fascination with how close we could push signals to the theoretical Shannon limit. That era demanded that you understand systems from microcode all the way up to the orbital link budget. I even drafted my home Atari computer into service on the lab bench, leveraging its MOS Technology 6502 architecture to write assembly language and develop code for a 65C102-driven phase-locked loop destined for satellite tracking and communications.

My work centered largely on error correction and high-speed signal processing. I co-patented a hardware implementation of serial-architecture Viterbi algorithm decoders, translating the complex mathematics of Comsat's brilliant theorists into physical hardware - first using discrete TTL and programmable logic arrays (PLAs). As bandwidth demands soared, we pushed the envelope by designing a blazing-fast Add-Compare-Select (ACS) engine, the notorious bottleneck in any Viterbi processor. We initially built it as a dense 3"x3" hybrid circuit, bonding Gallium Arsenide emitter-coupled logic (ECL) die directly onto a single substrate and having it radiation-hardened for spaceflight. Because those hybrid modules generated substantial heat and required elaborate cooling systems, the next logical step was integrating the entire architecture onto a custom array, such as the Motorola Gallium Arsenide (GaAs) gate array.
However, Motorola's own semi-automated place-and-route tools choked on the timing constraints; their software simply couldn't hit our required clock speeds, even though our engineering intuition promised it was physically achievable. Refusing to let the silicon stall, I dove into Donald Knuth's seminal texts on algorithms - focusing on the traveling salesman problem and combinatorial heuristics - sat down with Borland Turbo C on my personal IBM PC, and authored a custom routing suite from scratch. It successfully mapped the layout and closed timing on the gate array. With Comsat's blessing, I handed the software to Motorola at their eager request.

Perhaps the most satisfying achievement came when I spearheaded a project to dramatically overhaul satellite channel capacity without demanding any extra spectrum. By repurposing state-of-the-art commercial Reed-Solomon chips - designed and used in hard drive error correction - and pairing them with an Analog Devices ADSP-2100 series DSP, I architected an inline Reed-Solomon CODEC for Intermediate Data Rate (IDR) satellite modems. A minor tweak to the modem's digital shaping filters and the insertion of that codec into the baseband data stream

slashed bit error rates by several orders of magnitude. Proving it meant taking the hardware out of Clarksburg and into the field: I traveled to Earth stations in England for trans-Atlantic live-link testing, and to Thailand to validate it across the Pacific. Both trials were highly successful. Seeing hardware and software that began on a workbench in Clarksburg survive global field trials and become adopted into international satellite standards - still quietly operating decades later - remains one of the proudest legacies of my career.